NOVEMBER 1969

AWM1268

FOUR-BIT MEMORY Serial in, parallel out

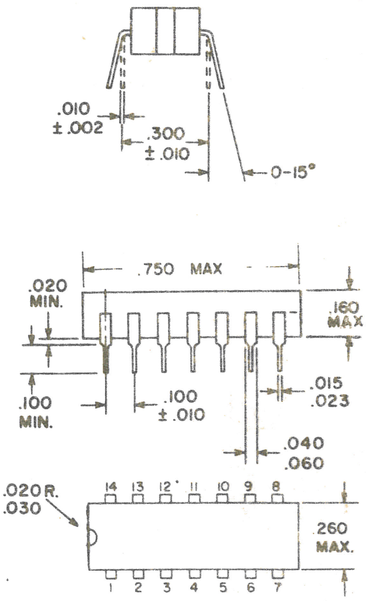
DESCRIPTION

The AWM 1268 is a DTL MSI functional block incorporating a four-bit store. Input data is applied on a common line and entry to a cell is enabled by the negative-going edge of a clock pulse on the appropriate write enable line. The edge triggered write mode is provided by a master-slave flip-flop. The output of each of the four cells is buffered onto an open-collector output stage, providing a wired-OR capability. Outputs may read from any cell independently of data entry.

GENERAL CHARACTERISTICS

Package:	14 pin hermetic Dual-in-line ceramic
Max. storage temp:	140°C
Operating temp. range:	0°C to 70°C
Supply voltage range:	4.5 to 5.5V
Max. input to any pin:	+5.5V
Min. input to any pin:	-0.5V
Logic Levels:	Compatible with TTL/DTL
Fan out (per line):	2 standard loads
Write cycle time:	45ns (typical)
Power dissipation:	150mW

DIMENSIONAL OUTLINE



(Dimensions in Inches)

PIN CONNECTIONS

1. Ground
2. V_{CC}
3. Read Cell 4
4. Read Cell 3
5. Read Cell 2
6. Read Cell 1
7. V_{CC}
8. Ground
9. Data in
10. Write Cell 1
11. Write Cell 2
12. Write Cell 3
13. Write Cell 4
14. Data in

Pins 1-8, 2-7, 9-14 are connected internally

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INTEGRATED CIRCUIT

AWV PRIVATE MAIL BAG ERMINGTON 2115 TELEGRAMS "VALVES" ERMINGTON TELEPHONE 638 0411

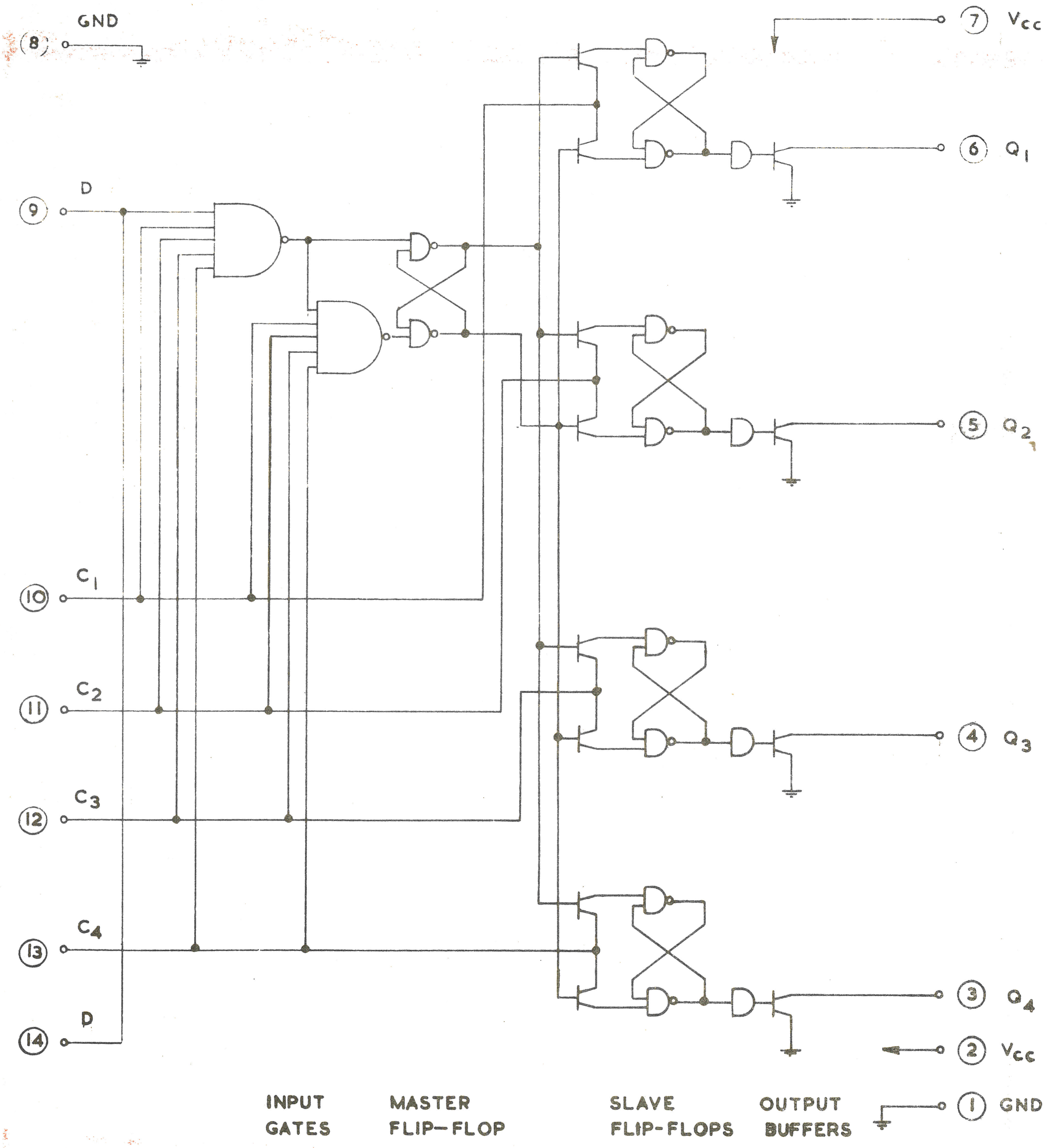


FIGURE 1 AWM 1268 FUNCTIONAL SCHEMATIC

PIN	FUNCTION	PARAMETER ($T= 25^{o}C$)	FORCING FUNCTION	LIMITS			UNITS
				MIN	TYP	MAX	
1	Ground[1] (Common with 8)						
2	Positive[1] Supply (Common with 7)	Voltage (V_{CC}) Current	 V_{CC}= 5.0V	+4.5 20	5.0 25	5.5 35	V mA
3	Output (Q4) Cell 4	High state current Low state voltage(V_{OL})	V_{OH}= 5.0V I_{Load}=2mA	0 .25	 .35	0.01 .40	mA V
4	Output[2] (Q_3) Cell 3	See (3)					
5	Output (Q_2) Cell 2	See (3)					
6	Output (Q_1) Cell 1	See (3)					
7	Positive supply[1] (Common with 2)	See (2)					
8	Ground[1] (Common with 1)						
9	Data in[1] (D) (Common with14)	Low state: Voltage V_{IL} Current I_{IL} High state: voltage V_{IH} Current I_{IH}	 V_{IL}=0 V V_{IH}=5.0 V	 -.5 -1.0 2.0 0	 -1.4 	 1.4 -2 5.5 .01	 V mA V mA
10	Write clock[3](C_1) Cell 1	Low state: voltage V_{IL} current High state: voltage V_{IH} current	 V_{IL}=0 V V_{IH}=5.0 V	 -.5 -3 2 0	 -4.5 	 0.8 -5.5 5.5 0.1	 V mA V mA
11	Write clock(C_2) Cell 2	See (10)					
12	Write clock(C_3) Cell 3	See (10)					
13	Write clock(C_4) Cell 4	See (10)					
14	Data in[1](D) (Common with 9)	See (9)					

Notes

1. It is recommended that common pins be externally shorted.
2. Q outputs are non-inverted with respect to D. External pull-up resistors should be used to define the high-state voltage level.
3. On a negative-going clock pulse, the data entry gates are disabled at V_I = 1.4V and data transfer to the store (slave) flip flops is enabled for V_I = 0.8V.

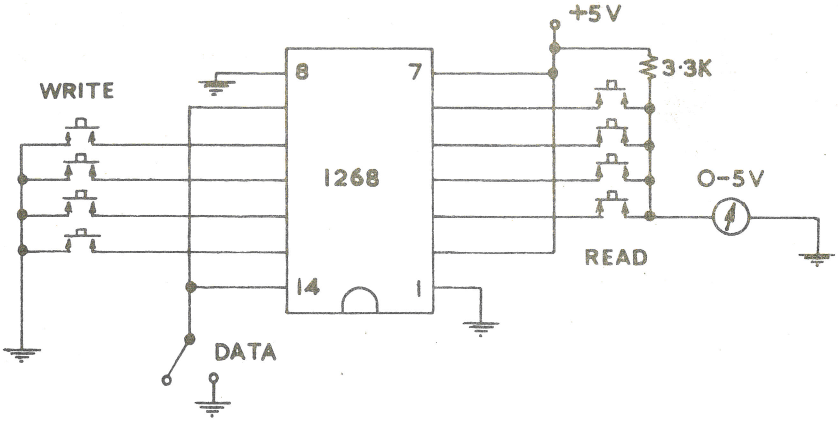
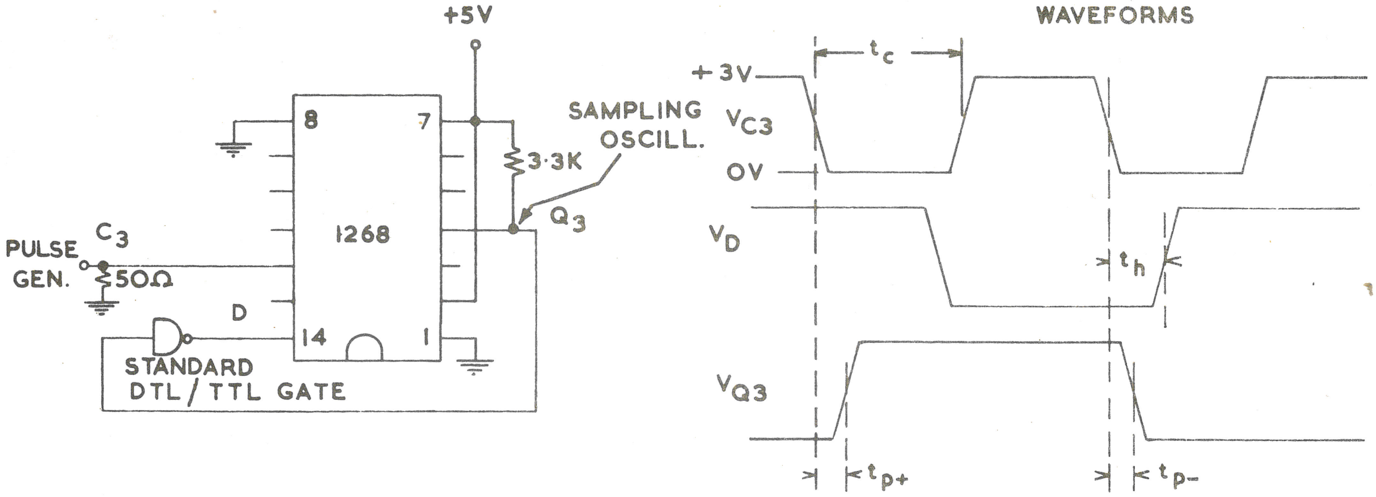


FIGURE 2 FUNCTIONAL TEST SET-UP



TYPICAL SWITCHING PARAMETERS

MINIMUM NEGATIVE CLOCK DURATION	t_c	40ns
FULL PROPOGATION TIME	t_{p+}	40ns
	t_{p-}	25ns
DATA SET-UP TIME	t_{ds}	35ns
DATA HOLD TIME	t_h	15ns

FIGURE 3 SPEED TEST SET-UP

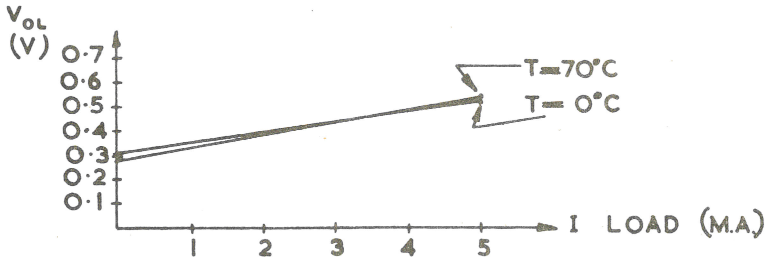


FIGURE 4 OUTPUT LOADING CURVE (LOW STATE)